9-Mbit (256K x 32) Pipelined DCD Sync SRAM

Features

- **Registered inputs and outputs for pipelined operation**
- **Optimal for performance (Double-Cycle deselect)**
  - **— Depth expansion without wait state**
- **256K × 32-bit common I/O architecture**
- **3.3V core power supply (V_{DD})**
- **2.5V/3.3V I/O power supply (V_{DDQ})**
- **Fast clock-to-output times**
  - **— 2.8 ns (for 250-MHz device)**
- **Provide high-performance 3-1-1-1 access rate**
- **User-selectable burst counter supporting Intel® Pentium® interleaved or linear burst sequences**
- **Multiple chip enables for depth expansion: Three chip enables for A package version and Two chip enables for AJ package version**
- **Separate processor and controller address strobes**
- **Synchronous self-timed writes**
- **Asynchronous Output Enable**
- **Available in JEDEC-standard lead-free 100-Pin TQFP package**
- **"ZZ" Sleep Mode option**

Functional Description[1]

The CY7C1368C SRAM integrates 256K x 32 SRAM cells with advanced synchronous peripheral circuitry and a two-bit counter for internal burst operation. All synchronous inputs are gated by registers controlled by a positive-edge-triggered Clock Input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining Chip Enable ($\overline{CE_1}$), depth-expansion Chip Enables (CE_2 and $\overline{CE_3}$[2]), Burst Control inputs ($\overline{ADSC}$, $\overline{ADSP}$, and $\overline{ADV}$), Write Enables ($\overline{BW_A}$, $\overline{BW_B}$, $\overline{BW_C}$, $\overline{BW_D}$, and $\overline{BWE}$), and Global Write ($\overline{GW}$). Asynchronous inputs include the Output Enable ($\overline{OE}$) and the ZZ pin.

Addresses and chip enables are registered at rising edge of clock when either Address Strobe Processor ($\overline{ADSP}$) or Address Strobe Controller ($\overline{ADSC}$) are active. Subsequent burst addresses can be internally generated as controlled by the Advance pin ($\overline{ADV}$).

Address, data inputs, and write controls are registered on-chip to initiate a self-timed Write cycle. This part supports Byte Write operations (see Pin Descriptions and Truth Table for further details). Write cycles can be one to four bytes wide as controlled by the byte write control inputs. $\overline{GW}$ active LOW causes all bytes to be written. This device incorporates an additional pipelined enable register which delays turning off the output buffers an additional cycle when a deselect is executed.This feature allows depth expansion without penal izing system performance.

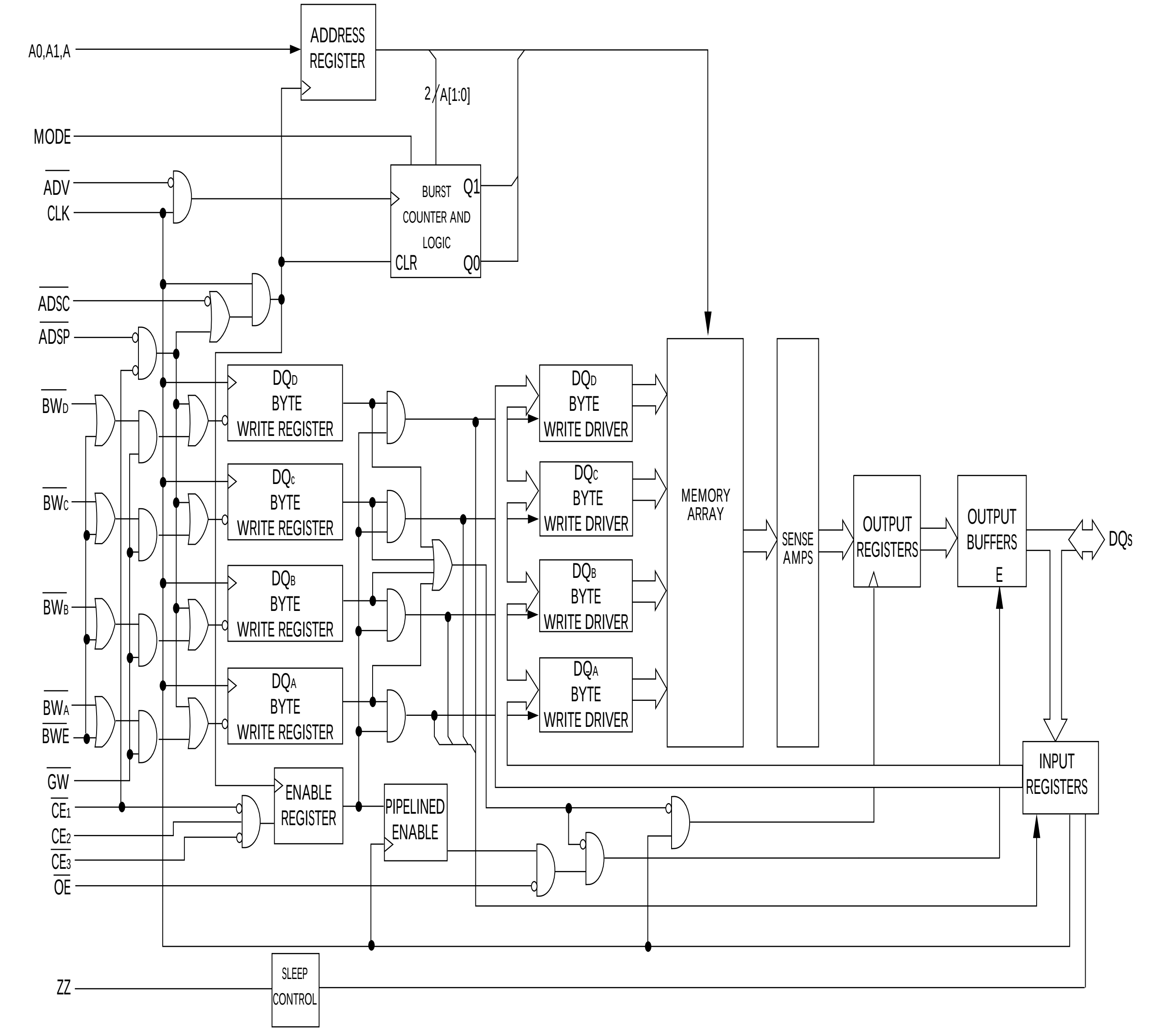
The CY7C1368C operates from a +3.3V core power supply while all outputs may operate with either a +2.5 or +3.3V supply. All inputs and outputs are JEDEC-standard JESD8-5-compatible.

Selection Guide

	250 MHz	200 MHz	166 MHz	Unit
Maximum Access Time	2.8	3.0	3.5	ns
Maximum Operating Current	250	220	180	mA
Maximum CMOS Standby Current	40	40	40	mA

Notes:
1. For best-practice recommendations, please refer to the Cypress application note *System Design Guidelines* on http://www.cypress.com.
2. $\overline{CE_3}$ is for A version (3 Chip enable option) only.

Functional Block Diagram-CY7C1368C (256K x 32)

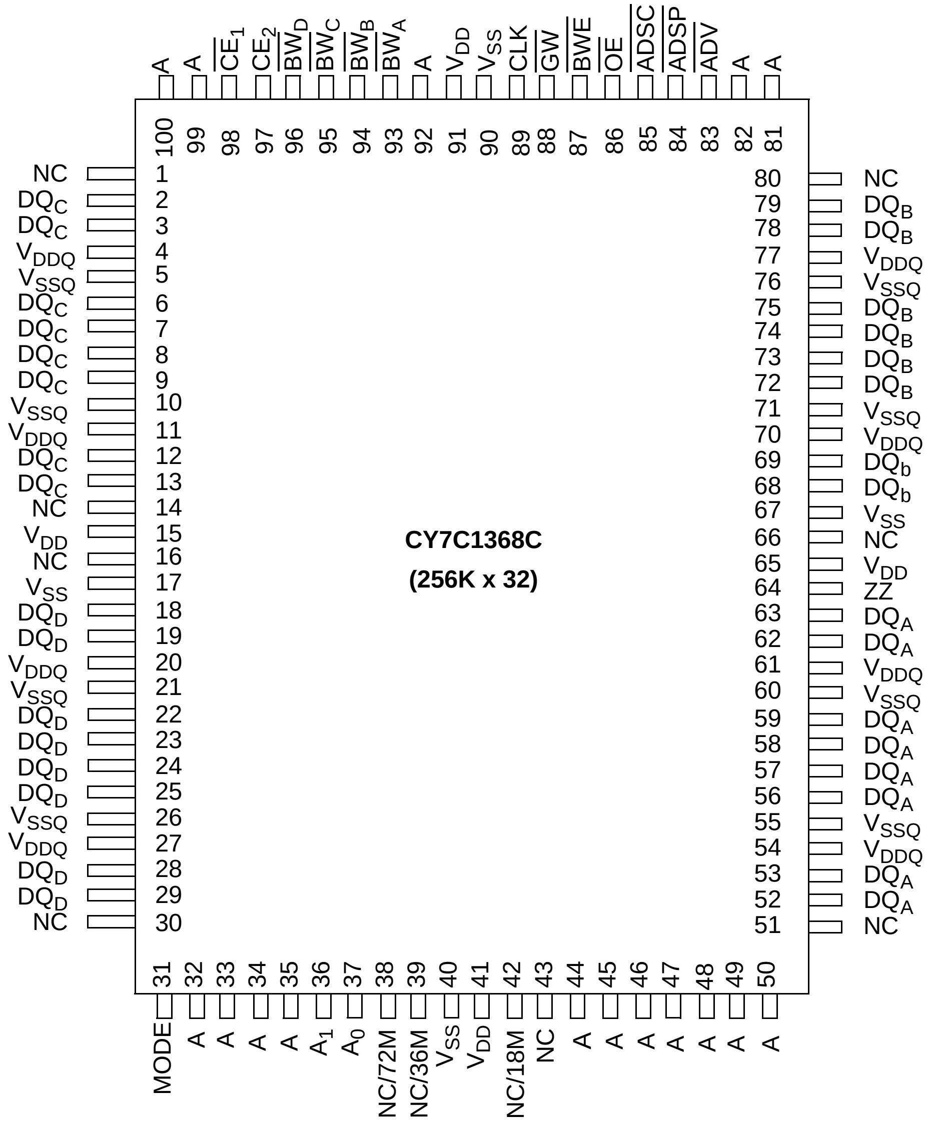


[+] Feedback

Pin Configurations

100-Pin TQFP Pinout (2-Chip Enable) (AJ version)

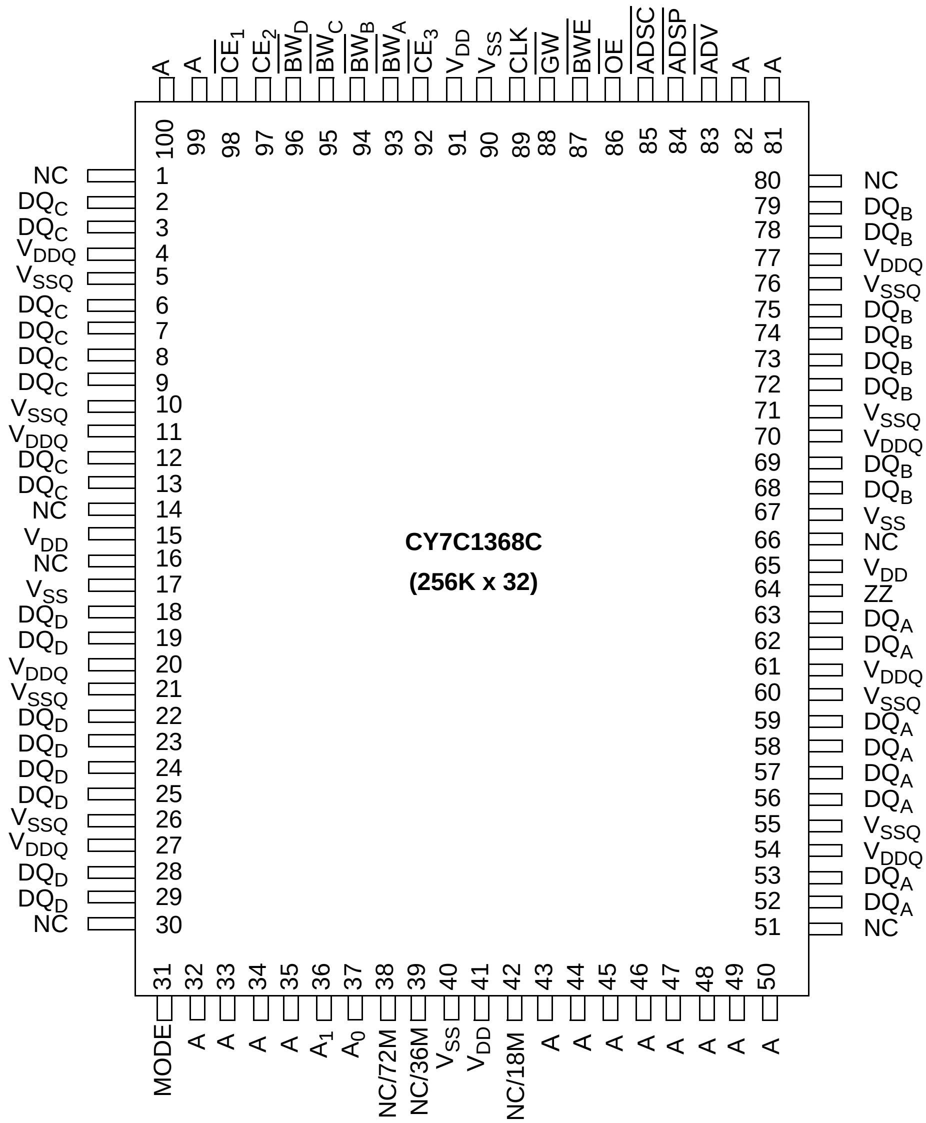
Top View



Pin Configurations (continued)

100-Pin TQFP Pinout (3-Chip Enable) (A version)

Top View



Pin Descriptions

Pin	TQFP	Type	Description
A_0, A_1, A	37, 36, 32, 33, 34, 35, 44, 45, 46, 47, 48, 49, 50, 80, 81, 82, 99, 100, 92 (AJC), 43 (AC)	Input-Synchronous	**Address Inputs used to select one of the 256K address locations**. Sampled at the rising edge of the CLK if $\overline{\text{ADSP}}$ or $\overline{\text{ADSC}}$ is active LOW, and $\overline{\text{CE}}_1$, CE_2, and $\overline{\text{CE}}_3$[2] are sampled active. $A_{[1:0]}$ are fed to the two-bit counter.
$\overline{\text{BW}}_A$, $\overline{\text{BW}}_B$, $\overline{\text{BW}}_C$, $\overline{\text{BW}}_D$	93, 94	Input-Synchronous	**Byte Write Select Inputs, active LOW**. Qualified with $\overline{\text{BWE}}$ to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{\text{GW}}$	88	Input-Synchronous	**Global Write Enable Input, active LOW**. When asserted LOW on the rising edge of CLK, a global write is conducted (ALL bytes are written, regardless of the values on $\overline{\text{BW}}_{[A:D]}$ and $\overline{\text{BWE}}$).
$\overline{\text{BWE}}$	87	Input-Synchronous	**Byte Write Enable Input, active LOW**. Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
CLK	89	Input-Clock	**Clock Input**. Used to capture all synchronous inputs to the device. Also used to increment the burst counter when $\overline{\text{ADV}}$ is asserted LOW, during a burst operation.
$\overline{\text{CE}}_1$	98	Input-Synchronous	**Chip Enable 1 Input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{\text{CE}}_3$ to select/deselect the device. $\overline{\text{ADSP}}$ is ignored if $\overline{\text{CE}}_1$ is HIGH. $\overline{\text{CE}}_1$ is sampled only when a new external address is loaded.
CE_2	97	Input-Synchronous	**Chip Enable 2 Input, active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{\text{CE}}_1$ and $\overline{\text{CE}}_3$ to select/deselect the device. CE_2 is sampled only when a new external address is loaded.
$\overline{\text{CE}}_3$[2]	92	Input-Synchronous	**Chip Enable 3 Input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{\text{CE}}_1$ and CE_2 to select/deselect the device. Not available for AJ package version.$\overline{\text{CE}}_3$[2] is assumed active throughout this document for BGA. $\overline{\text{CE}}_3$ is sampled only when a new external address is loaded.
$\overline{\text{OE}}$	86	Input-Asynchronous	**Output Enable, asynchronous input, active LOW**. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins. $\overline{\text{OE}}$ is masked during the first clock of a read cycle when emerging from a deselected state.
$\overline{\text{ADV}}$	83	Input-Synchronous	**Advance Input signal, sampled on the rising edge of CLK, active LOW**. When asserted, it automatically increments the address in a burst cycle.
$\overline{\text{ADSP}}$	84	Input-Synchronous	**Address Strobe from Processor, sampled on the rising edge of CLK, active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When $\overline{\text{ADSP}}$ and $\overline{\text{ADSC}}$ are both asserted, only $\overline{\text{ADSP}}$ is recognized. $\overline{\text{ASDP}}$ is ignored when $\overline{\text{CE}}_1$ is deasserted HIGH.
$\overline{\text{ADSC}}$	85	Input-Synchronous	**Address Strobe from Controller, sampled on the rising edge of CLK, active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When $\overline{\text{ADSP}}$ and $\overline{\text{ADSC}}$ are both asserted, only $\overline{\text{ADSP}}$ is recognized.
ZZ	64	Input-Asynchronous	**ZZ “sleep” Input, active HIGH**. When asserted HIGH places the device in a non-time-critical “sleep” condition with data integrity preserved. For normal operation, this pin has to be LOW or left floating. ZZ pin has an internal pull-down.
DQs	2, 3, 6, 7, 8, 9, 12, 13, 18, 19, 22, 23, 24, 25, 28, 29, 52, 53, 56, 57, 58, 59, 62, 63, 68, 69, 72, 73, 74, 75, 78, 79	I/O-Synchronous	**Bidirectional Data I/O lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{\text{OE}}$. When $\overline{\text{OE}}$ is asserted LOW, the pins behave as outputs. When HIGH, DQs are placed in a tri-state condition.
V_{DD}	15, 41, 65, 91	Power Supply	**Power supply inputs to the core of the device**.
V_{SS}	17, 40, 67, 90	Ground	**Ground for the core of the device**.

Pin Descriptions (continued)

Pin	TQFP	Type	Description
V_{DDQ}	4, 11, 20, 27, 54, 61, 70, 77	I/O Power Supply	**Power supply for the I/O circuitry**.
V_{SSQ}	5, 10, 21, 26, 55, 60, 71, 76	I/O Ground	**Ground for the I/O circuitry**.
MODE	31	Input-Static	**Selects Burst Order**. When tied to GND selects linear burst sequence. When tied to V_{DD} or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation. Mode Pin has an internal pull-up.
NC	1, 16, 30, 38, 39, 42, 43(AJC), 51, 66, 80		**No Connects**. Not internally connected to the die. NC/(18M,36M, 72M, 144M, 288M, 576M, 1G) **These pins are not connected**. They will be used for expansion to the 18M, 36M, 72M, 144M, 288M, 576M and 1G densities.

Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock.

The CY7C1368C supports secondary cache in systems utilizing either a linear or interleaved burst sequence. The interleaved burst order supports Pentium and i486™ processors. The linear burst sequence is suited for processors that utilize a linear burst sequence. The burst order is user selectable, and is determined by sampling the MODE input. Accesses can be initiated with either the Processor Address Strobe ($\overline{ADSP}$) or the Controller Address Strobe ($\overline{ADSC}$). Address advancement through the burst sequence is controlled by the $\overline{ADV}$ input. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the Byte Write Enable ($\overline{BWE}$) and Byte Write Select ($\overline{BW}_{[A:D]}$) inputs. A Global Write Enable ($\overline{GW}$) overrides all byte write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self-timed write circuitry.

Synchronous Chip Selects $\overline{CE}_1$, CE_2, $\overline{CE}_3$ and an asynchronous Output Enable ($\overline{OE}$) provide for easy bank selection and output tri-state control. $\overline{ADSP}$ is ignored if $\overline{CE}_1$ is HIGH.

Single Read Accesses

This access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{ADSP}$ or $\overline{ADSC}$ is asserted LOW, (2) chip selects are all asserted active, and (3) the write signals ($\overline{GW}$, $\overline{BWE}$) are all deasserted HIGH. $\overline{ADSP}$ is ignored if $\overline{CE}_1$ is HIGH. The address presented to the address inputs is stored into the address advancement logic and the Address Register while being presented to the memory core. The corresponding data is allowed to propagate to the input of the Output Registers. At the rising edge of the next clock the data is allowed to propagate through the output register and onto the data bus within t_{co} if $\overline{OE}$ is active LOW. The only exception occurs when the SRAM is emerging from a deselected state to a selected state, its outputs are always tri-stated during the first cycle of the access. After the first cycle of the access, the outputs are controlled by the $\overline{OE}$ signal. Consecutive single read cycles are supported.

The CY7C1368C is a double-cycle deselect part. Once the SRAM is deselected at clock rise by the chip select and either $\overline{ADSP}$ or $\overline{ADSC}$ signals, its output will tri-state immediately after the next clock rise.

Single Write Accesses Initiated by $\overline{ADSP}$

This access is initiated when both of the following conditions are satisfied at clock rise: (1) $\overline{ADSP}$ is asserted LOW, and (2) chip select is asserted active. The address presented is loaded into the address register and the address advancement logic while being delivered to the memory core. The write signals ($\overline{GW}$, $\overline{BWE}$, and $\overline{BW}_{[A:D]}$) and $\overline{ADV}$ inputs are ignored during this first cycle.

$\overline{ADSP}$ triggered write accesses require two clock cycles to complete. If $\overline{GW}$ is asserted LOW on the second clock rise, the data presented to the DQx inputs is written into the corresponding address location in the memory core. If $\overline{GW}$ is HIGH, then the write operation is controlled by $\overline{BWE}$ and $\overline{BW}_{[A:D]}$ signals. The CY7C1368C provides byte write capability that is described in the Write Cycle Description table. Asserting the Byte Write Enable input ($\overline{BWE}$) with the selected Byte Write input will selectively write to only the desired bytes. Bytes not selected during a byte write operation will remain unaltered. A synchronous self-timed write mechanism has been provided to simplify the write operations.

Because the CY7C1368C is a common I/O device, the Output Enable ($\overline{OE}$) must be deasserted HIGH before presenting data to the DQ inputs. Doing so will tri-state the output drivers. As a safety precaution, DQs are automatically tri-stated whenever a write cycle is detected, regardless of the state of $\overline{OE}$.

Single Write Accesses Initiated by $\overline{ADSC}$

$\overline{ADSC}$ write accesses are initiated when the following conditions are satisfied: (1) $\overline{ADSC}$ is asserted LOW, (2) $\overline{ADSP}$ is deasserted HIGH, (3) chip select is asserted active, and (4) the appropriate combination of the write inputs ($\overline{GW}$, $\overline{BWE}$, and $\overline{BW}_{[A:D]}$) are asserted active to conduct a write to the desired byte(s). $\overline{ADSC}$ triggered write accesses require a single clock cycle to complete. The address presented is loaded into the address register and the address advancement logic while being delivered to the memory core. The $\overline{ADV}$ input is ignored during this cycle. If a global write is conducted, the data presented to the DQ_X is written into the corresponding address location in the memory core. If a byte write is conducted, only the selected bytes are written. Bytes not selected during a byte write operation will remain unaltered. A synchronous self-timed write mechanism has been provided to simplify the write operations.

Because the CY7C1368C is a common I/O device, the Output Enable ($\overline{OE}$) must be deasserted HIGH before presenting data to the DQ_X inputs. Doing so will tri-state the output drivers. As a safety precaution, DQ_X are automatically tri-stated whenever a write cycle is detected, regardless of the state of $\overline{OE}$.

Burst Sequences

The CY7C1368C provides a two-bit wraparound counter, fed by $A_{[1:0]}$, that implements either an interleaved or linear burst sequence. The interleaved burst sequence is designed specifically to support Intel Pentium applications. The linear burst sequence is designed to support processors that follow a linear burst sequence. The burst sequence is user selectable through the MODE input. Both read and write burst operations are supported

Asserting $\overline{ADV}$ LOW at clock rise will automatically increment the burst counter to the next address in the burst sequence. Both read and write burst operations are supported.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation "sleep" mode. Two clock cycles are required to enter into or exit from this "sleep" mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the "sleep" mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the "sleep" mode. $\overline{CE}$s, $\overline{ADSP}$, and $\overline{ADSC}$ must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

Interleaved Burst Address Table

(MODE = Floating or V_{DD})

First Address A1, A0	Second Address A1, A0	Third Address A1, A0	Fourth Address A1, A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Address Table (MODE = GND)

First Address A1, A0	Second Address A1, A0	Third Address A1, A0	Fourth Address A1, A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

Truth Table[3, 4, 5, 6, 7]

Operation	Address Used	$\overline{CE_1}$	$\overline{CE_3}$	CE_2	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected Cycle, Power-down	None	H	X	X	L	X	L	X	X	X	L-H	Tri-state
Deselected Cycle, Power-down	None	L	X	L	L	L	X	X	X	X	L-H	Tri-state
Deselected Cycle, Power-down	None	L	H	X	L	L	X	X	X	X	L-H	Tri-state
Deselected Cycle, Power-down	None	L	X	L	L	H	L	X	X	X	L-H	Tri-state
Deselected Cycle, Power-down	None	L	H	X	L	H	L	X	X	X	L-H	Tri-state
ZZ Mode, Power-down	None	X	X	X	H	X	X	X	X	X	X	Tri-state
Read Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	L	L-H	Q
Read Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	H	L-H	Tri-state
Write Cycle, Begin Burst	External	L	L	H	L	H	L	X	L	X	L-H	D
Read Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	L	L-H	Q
Read Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	H	L-H	Tri-state
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q

Notes:

3. X = "Don't Care." H = Logic HIGH, L =Logic LOW.
4. $\overline{WRITE}$ = L when any one or more Byte Write enable signals ($\overline{BW_A}$, $\overline{BW_B}$, $\overline{BW_C}$, $\overline{BW_D}$) and $\overline{BWE}$ = L or $\overline{GW}$ = L. $\overline{WRITE}$ = H when all Byte write enable signals (BW_A, BW_B, BW_C, BW_D), BWE, GW=H.
5. The DQ pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.
6. The SRAM always initiates a read cycle when $\overline{ADSP}$ is asserted, regardless of the state of $\overline{GW}$, $\overline{BWE}$, or $\overline{BW_{[A:D]}}$. Writes may occur only on subsequent clocks after the $\overline{ADSP}$ or with the assertion of $\overline{ADSC}$. As a result, $\overline{OE}$ must be driven HIGH prior to the start of the write cycle to allow the outputs to tri-state. $\overline{OE}$ is a don't care for the remainder of the write cycle.
7. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle all data bits are Tri-State when $\overline{OE}$ is inactive or when the device is deselected, and all data bits behave as output when $\overline{OE}$ is active (LOW).

Truth Table[3, 4, 5, 6, 7] (continued)

Operation	Address Used	$\overline{CE_1}$	$\overline{CE_3}$	CE_2	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L-H	Tri-state
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L-H	Tri-state
Write Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L-H	D
Write Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L-H	Tri-state
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L-H	Tri-state
Write Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
Write Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

Truth Table for Read/Write[3, 4]

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_A}$	$\overline{BW_B}$	$\overline{BW_C}$	$\overline{BW_D}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write byte A - (DQ_A and DQP_A)	H	L	L	H	H	H
Write byte B - (DQ_B and DQP_B)	H	L	H	L	H	H
Write byte C - (DQ_C and DQP_C)	H	L	H	H	L	H
Write byte D - (DQ_D and DQP_D)	H	L	H	H	H	L
Write all bytes	H	L	L	L	L	L
Write all bytes	L	X	X	X	X	X

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min.	Max.	Unit
I_{DDZZ}	sleep mode standby current	$ZZ \geq V_{DD} - 0.2V$		50	mA
t_{ZZS}	Device operation to ZZ	$ZZ \geq V_{DD} - 0.2V$		$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	$ZZ \leq 0.2V$	$2t_{CYC}$		ns
t_{ZZI}	ZZ recovery time	This parameter is sampled		$2t_{CYC}$	ns
t_{RZZI}	ZZ inactive to exit sleep current	This parameter is sampled	0		ns

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... –65°C to +150°

Ambient Temperature with Power Applied..–55°C to +125°C

Supply Voltage on V_{DD} Relative to GND........ –0.5V to +4.6V

Supply Voltage on V_{DDQ} Relative to GND ...... –0.5V to $+V_{DD}$

DC Voltage Applied to Outputs in Tri-State .... –0.5V to V_{DDQ} +0.5V

DC Input Voltage .... –0.5V to V_{DD}+0.5V

Current into Outputs (LOW).. 20 mA

Static Discharge Voltage... >2001V

(per MIL-STD-883,Method 3015)

Latch-up Current... >200 mA

Operating Range

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	3.3V – 5%/+10%	2.5V – 5% to V_{DD}
Industrial	–40°C to +85°C		

Electrical Characteristics Over the Operating Range[8, 9]

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{DD}	Power Supply Voltage			3.135	3.6	V
V_{DDQ}	I/O Supply Voltage	for 3.3V I/O		3.135	V_{DD}	V
		for 2.5V I/O		2.375	2.625	V
V_{OH}	Output HIGH Voltage	for 3.3V I/O, I_{OH} = –4.0 mA		2.4		V
		for 2.5V I/O, I_{OH} = –1.0 mA		2.0		V
V_{OL}	Output LOW Voltage	for 3.3V I/O, I_{OL} = 8.0 mA			0.4	V
		for 2.5V I/O, I_{OL} = 1.0 mA			0.4	V
V_{IH}	Input HIGH Voltage[8]	for 3.3V I/O		2.0	V_{DD} + 0.3V	V
		for 2.5V I/O		1.7	V_{DD} + 0.3V	V
V_{IL}	Input LOW Voltage[8]	for 3.3V I/O		–0.3	0.8	V
		for 2.5V I/O		–0.3	0.7	V
I_X	Input Leakage Current except ZZ and MODE	GND ≤ V_I ≤ V_{DDQ}		–5	5	µA
	Input Current of MODE	Input = V_{SS}		–30		µA
		Input = V_{DD}			5	µA
	Input Current of ZZ	Input = V_{SS}		–5		µA
		Input = V_{DD}			30	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ $V_{DDQ,}$ Output Disabled		–5	5	µA
I_{DD}	V_{DD} Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{CYC}$	4-ns cycle, 250 MHz		250	mA
			5-ns cycle, 200 MHz		220	mA
			6-ns cycle,166 MHz		180	mA
I_{SB1}	Automatic CE Power-down Current—TTL Inputs	V_{DD} = Max., Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX} = $1/t_{CYC}$	4-ns cycle, 250 MHz		130	mA
			5-ns cycle, 200 MHz		120	
			6-ns cycle,166 MHz		110	
I_{SB2}	Automatic CE Power-down Current—CMOS Inputs	V_{DD} = Max., Device Deselected, V_{IN} ≤ 0.3V or V_{IN} ≥ V_{DDQ} – 0.3V, f = 0	All speeds		40	mA
I_{SB3}	Automatic CE Power-down Current—CMOS Inputs	V_{DD} = Max., Device Deselected, or V_{IN} ≤ 0.3V or V_{IN} ≥ V_{DDQ} – 0.3V, f = f_{MAX} = $1/t_{CYC}$	4-ns cycle, 250 MHz		120	mA
			5-ns cycle, 200 MHz		110	
			6-ns cycle,166 MHz		100	
I_{SB4}	Automatic CE Power-down Current—TTL Inputs	V_{DD} = Max., Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = 0	All speeds		40	mA

Notes:

8. Overshoot: V_{IH}(AC) < V_{DD}+1.5V(Pulse width less than t_{CYC}/2), undershoot: V_{IL}(AC)> –2V(Pulse width less than t_{CYC}/2).
9. Power-up: Assumes a linear ramp from 0V to V_{DD}(min.) within 200 ms. During this time V_{IH} < V_{DD} and V_{DDQ} ≤ V_{DD}.

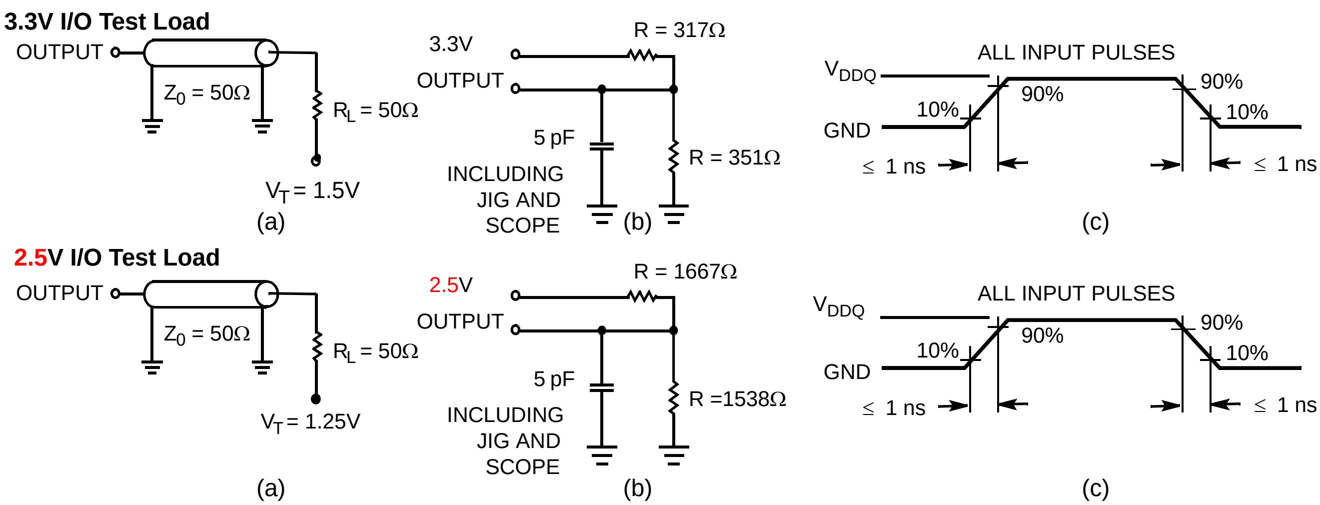
Capacitance[10]

Parameter	Description	Test Conditions	100 TQFP Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V V_{DDQ} = 2.5V	4	pF
C_{CLK}	Clock Input Capacitance		4	pF
$C_{I/O}$	Input/Output Capacitance		4	pF

Thermal Characteristics[10]

Parameter	Description	Test Conditions	100 TQFP Package	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51	29.41	°C/W
Θ_{JC}	Thermal Resistance (Junction to case)		6.13	°C/W

AC Test Loads and Waveforms



Note:
10. Tested initially and after any design or process change that may affect these parameters

Switching Characteristics Over the Operating Range [15, 16]

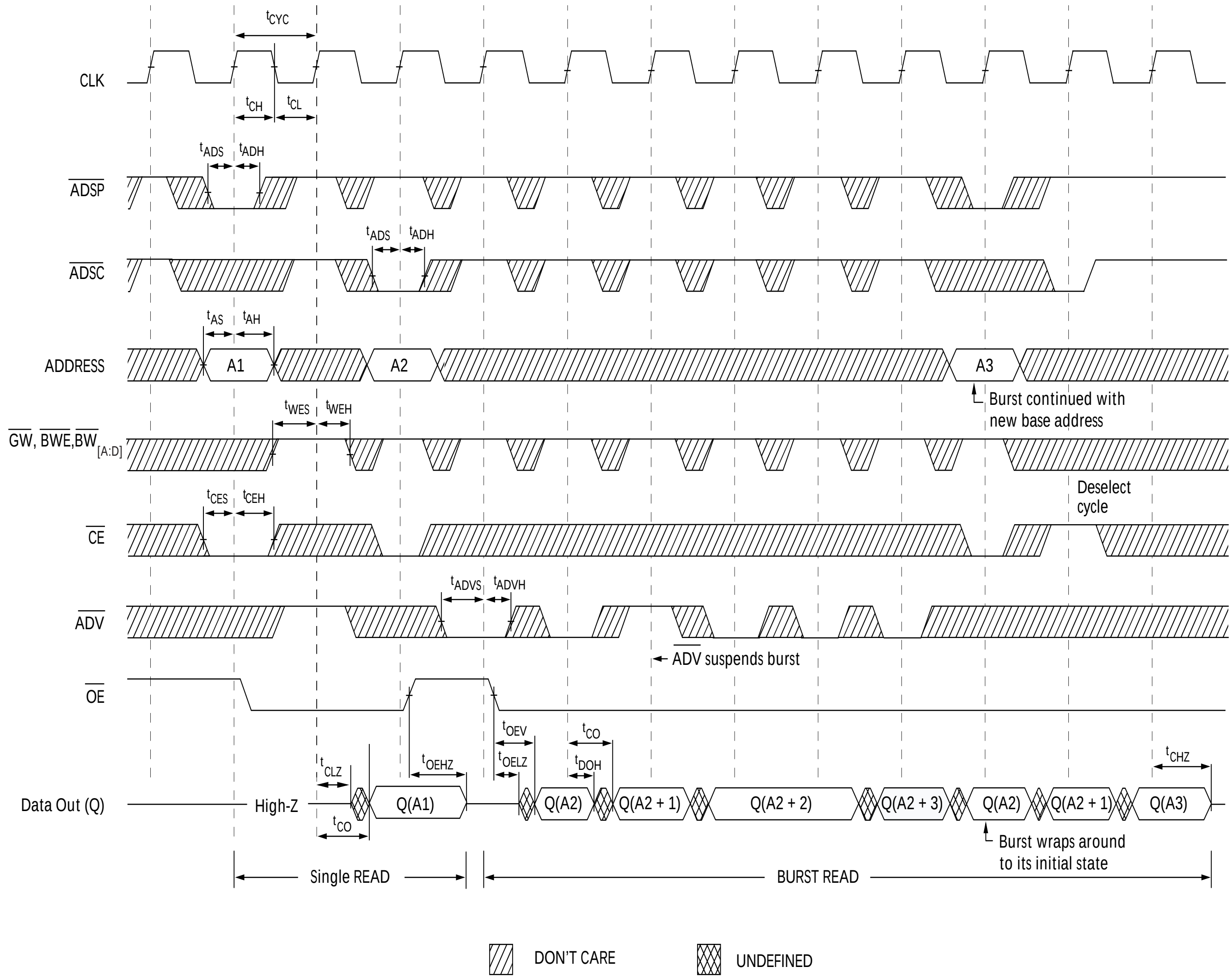
Parameter	Description	–250		–200		–166		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{POWER}	V_{DD}(Typical) to the first Access[11]	1		1		1		ms
Clock								
t_{CYC}	Clock Cycle Time	4.0		5.0		6.0		ns
t_{CH}	Clock HIGH	1.8		2.0		2.4		ns
t_{CL}	Clock LOW	1.8		2.0		2.4		ns
Output Times								
t_{CO}	Data Output Valid After CLK Rise		2.8		3.0		3.5	ns
t_{DOH}	Data Output Hold After CLK Rise	1.25		1.25		1.25		ns
t_{CLZ}	Clock to Low-Z[12, 13, 14]	1.25		1.25		1.25		ns
t_{CHZ}	Clock to High-Z[12, 13, 14]	1.25	2.8	1.25	3.0	1.25	3.5	ns
t_{OEV}	$\overline{OE}$ LOW to Output Valid		2.8		3.0		3.5	ns
t_{OELZ}	$\overline{OE}$ LOW to Output Low-Z[12, 13, 14]	0		0		0		ns
t_{OEHZ}	$\overline{OE}$ HIGH to Output High-Z[12, 13, 14]		2.8		3.0		3.5	ns
Set-up Times								
t_{AS}	Address Set-up Before CLK Rise	1.4		1.5		1.5		ns
t_{ADS}	$\overline{ADSC}$, $\overline{ADSP}$ Set-up Before CLK Rise			1.5		1.5		ns
t_{ADVS}	$\overline{ADV}$ Set-up Before CLK Rise	1.4		1.5		1.5		ns
t_{WES}	$\overline{GW}$, $\overline{OE}$, $\overline{BW}_{[A:D]}$ Set-up Before CLK Rise	1.4		1.5		1.5		ns
t_{DS}	Data Input Set-up Before CLK Rise	1.4		1.5		1.5		ns
t_{CES}	Chip Enable Set-up Before CLK Rise	1.4		1.5		1.5		ns
Hold Times								
t_{AH}	Address Hold After CLK Rise	0.4		0.5		0.5		ns
t_{ADH}	$\overline{ADSP}$, $\overline{ADSC}$ Hold After CLK Rise	0.4		0.5		0.5		ns
t_{ADVH}	$\overline{ADV}$ Hold After CLK Rise	0.4		0.5		0.5		ns
t_{WEH}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW}_{[A:D]}$ Hold After CLK Rise	0.4		0.5		0.5		ns
t_{DH}	Data Input Hold After CLK Rise	0.4		0.5		0.5		ns
t_{CEH}	Chip Enable Hold After CLK Rise	0.4		0.5		0.5		ns

Notes:

11. This part has a voltage regulator internally; tpower is the time that the power needs to be supplied above V_{DD} minimum initially before a read or write operation can be initiated.
12. t_{CHZ}, t_{CLZ}, t_{OELZ}, and t_{OEHZ} are specified with AC test conditions shown in part (b) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
13. At any given voltage and temperature, t_{OEHZ} is less than t_{OELZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High-Z prior to Low-Z under the same system conditions.
14. This parameter is sampled and not 100% tested.
15. Timing reference level is 1.5V when V_{DDQ} = 3.3V and is 1.25 V when V_{DDQ} = 2.5 V.
16. Test conditions shown in (a) of AC Test Loads unless otherwise noted.

Switching Waveforms

Read Timing[17]

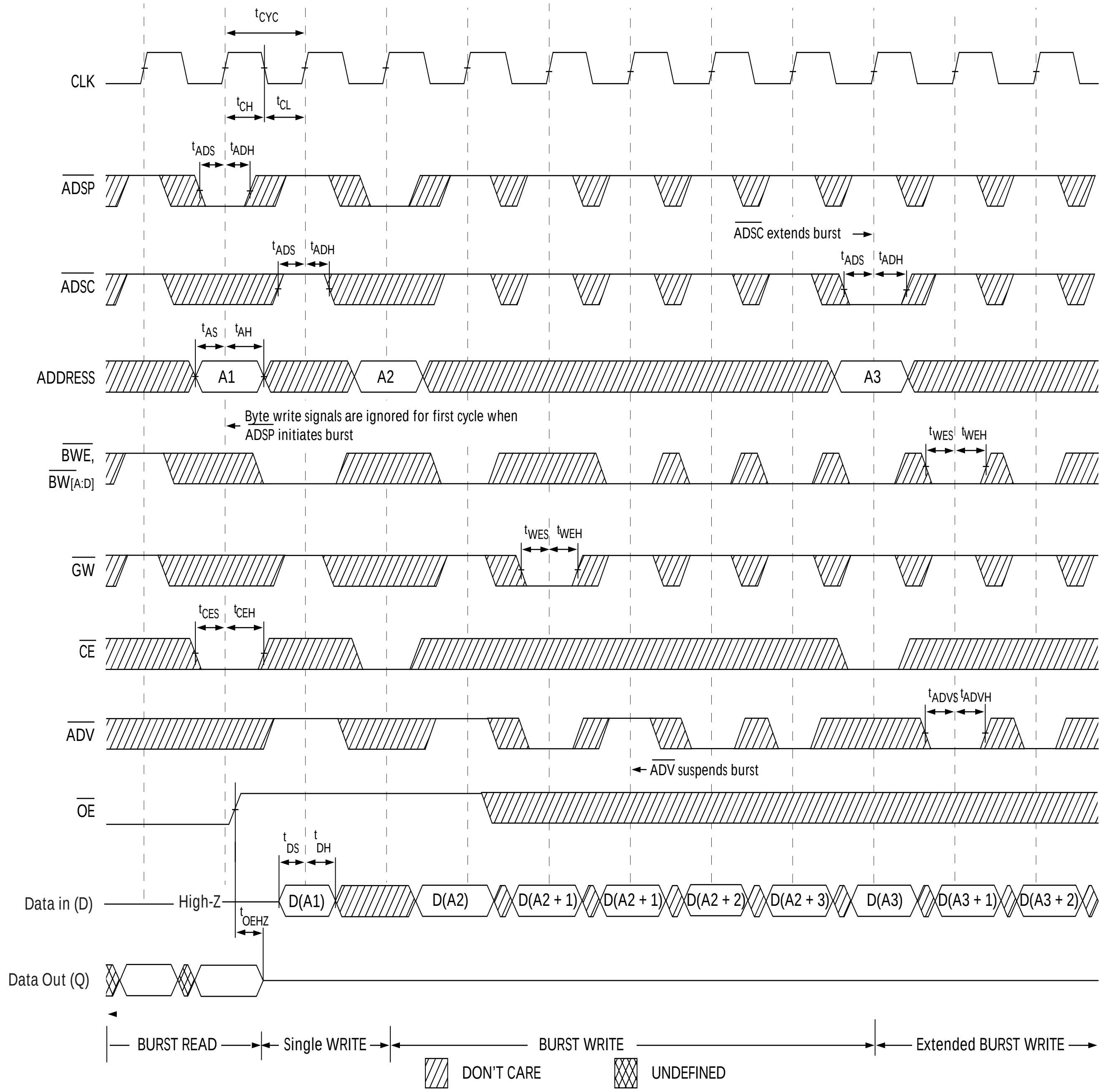


Note:

17. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.

Switching Waveforms (continued)

Write Timing[17, 18]

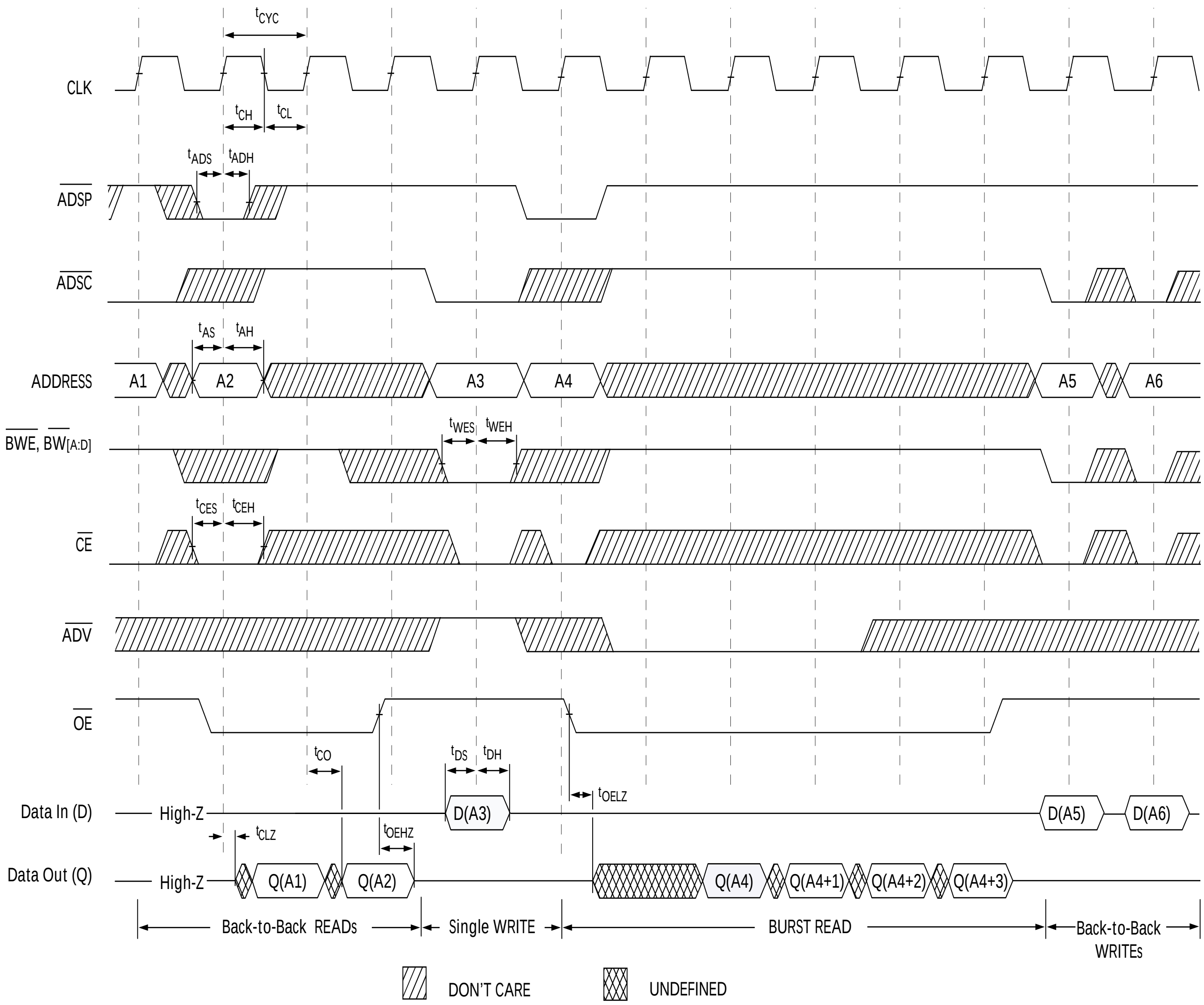


Note:

18. Full width write can be initiated by either $\overline{GW}$ LOW; or by $\overline{GW}$ HIGH, $\overline{BWE}$ LOW and $\overline{BW}_{[A:D]}$ LOW.

Switching Waveforms (continued)

Read/Write Timing[17, 19, 20]

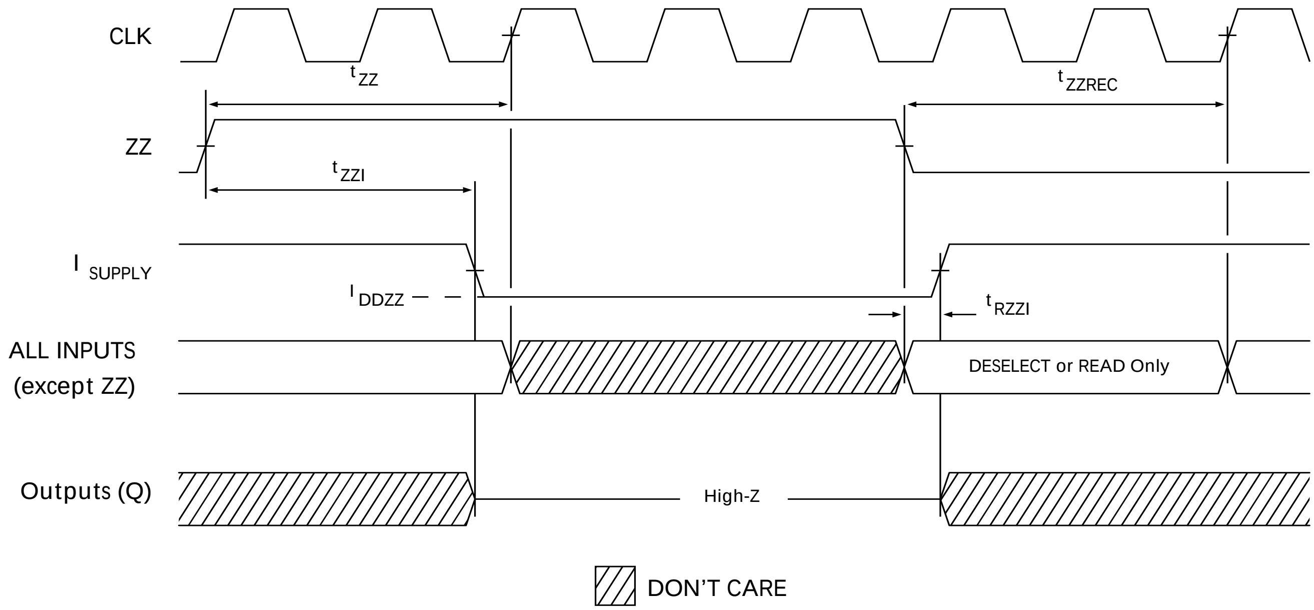


Notes:

19. The data bus (Q) remains in tri-state following a WRITE cycle unless a new read access is initiated by $\overline{\text{ADSP}}$ or $\overline{\text{ADSC}}$.
20. $\overline{\text{GW}}$ is HIGH.

Switching Waveforms (continued)

ZZ Mode Timing [21, 22.]



Notes:

21.Device must be deselected when entering ZZ mode. See truth table for all possible signal conditions to deselect the device.

22.DQs are in tri-state when exiting ZZ sleep mode.

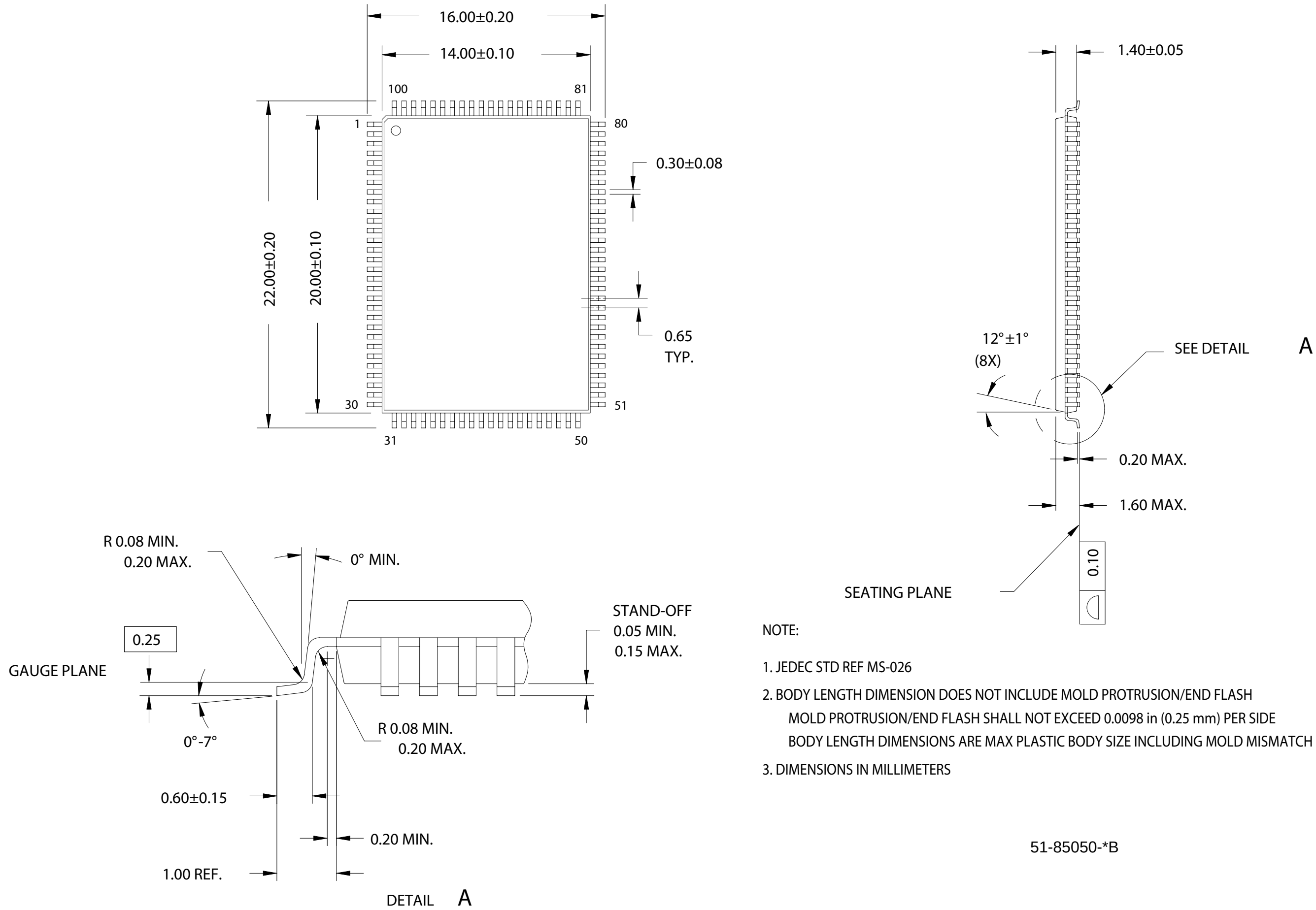
Ordering Information

Not all of the speed, package and temperature ranges are available. Please contact your local sales representative or visit www.cypress.com for actual products offered.

Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
166	CY7C1368C-166AXC	51-85050	100-pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Lead-Free (3 Chip enable)	Commercial
	CY7C1368C-166AJXC		100-pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Lead-Free (2 Chip enable)	
	CY7C1368C-166AXI		100-pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Lead-Free (3 Chip enable)	Industrial
	CY7C1368C-166AJXI		100-pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Lead-Free (2 Chip enable)	
200	CY7C1368C-200AXC	51-85050	100-pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Lead-Free (3 Chip enable)	Commercial
	CY7C1368C-200AJXC		100-pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Lead-Free (2 Chip enable)	
	CY7C1368C-200AXI		100-pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Lead-Free (3 Chip enable)	Industrial
	CY7C1368C-200AJXI		100-pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Lead-Free (2 Chip enable)	
250	CY7C1368C-250AXC	51-85050	100-pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Lead-Free (3 Chip enable)	Commercial
	CY7C1368C-250AJXC		100-pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Lead-Free (2 Chip enable)	
	CY7C1368C-250AXI		100-pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Lead-Free (3 Chip enable)	Industrial
	CY7C1368C-250AJXI		100-pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Lead-Free (2 Chip enable)	

Package Diagram

100-Pin TQFP (14 x 20 x 1.4 mm) (51-85050)



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Document History Page

Document Title: CY7C1368C 9-Mbit (256K x 32) Pipelined DCD Sync SRAM Document Number: 38-05686				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	286269	See ECN	PCI	New data sheet
*A	323636	See ECN	PCI	Changed frequency of 225 MHz to 250 MHz Added t_{CYC} to 4.0 ns for 250 MHz Changed Θ_{JA} and Θ_{JC} for TQFP Package from 25 and 9 °C/W to 29.41 and 6.13 °C/W respectively Added Industrial temperature range Replaced Snooze with Sleep in the ZZ Mode Electrical Characteristics Added 3 chip enable and 2 chip enable for AX and AJX packages in the ordering information table
*B	332879	See ECN	PCI	Shaded 250 MHz speed bin in the AC/DC Table and Selection Guide Added Address Expansion pins in the Pin Definition Table Modified V_{OL}, V_{OH} test conditions Corrected V_{DDQ} from (2.5V – 5% to V_{DD}) to (3.3V –5%/+10%) on page# 9 Updated Ordering Information Table
*C	377095	See ECN	PCI	Changed I_{SB2} from 30 to 40 mA Modified test condition in note# 9 from $V_{IH} \leq V_{DD}$ to $V_{IH} < V_{DD}$
*D	408725	See ECN	RXU	Changed address of Cypress Semiconductor Corporation on Page# 1 from “3901 North First Street” to “198 Champion Court” Converted from Preliminary to Final Replaced Package Name column with Package Diagram in the Ordering Information table Updated the ordering information
*E	429278	See ECN	NXR	Added 2.5VI/O option Updated Ordering Information Table
*F	501828	See ECN	VKN	Added the Maximum Rating for Supply Voltage on V_{DDQ} Relative to GND Updated the Ordering Information table.